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| APPLICATION NO.  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 10/775,222   | 02/11/2004  | Hirofumi Komori      | 1259-0243P          | 9988             |
| 2292   | 7590        | 06/16/2006           | EXAMINER            |                  |
| BIRCH STEWART KOLASCH & BIRCH<br>PO BOX 747<br>FALLS CHURCH, VA 22040-0747 |             |                      |                     | KRAIG, WILLIAM F |
|  |             |                      | ART UNIT            | PAPER NUMBER     |
|  |             |                      | 2815                |                  |

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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|                              |                        |                     |
|------------------------------|------------------------|---------------------|
| <b>Office Action Summary</b> | <b>Application No.</b> | <b>Applicant(s)</b> |
|                              | 10/775,222             | KOMORI, HIROFUMI    |
|                              | <b>Examiner</b>        | <b>Art Unit</b>     |
|                              | William Kraig          | 2815                |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 17 April 2006.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-15 is/are pending in the application.
  - 4a) Of the above claim(s) 10-13 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-9 is/are rejected.
- 7) Claim(s) 14 and 15 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 11 February 2004 is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____.   |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____.  | 6) <input type="checkbox"/> Other: _____.                                   |

## **DETAILED ACTION**

1. The addition of claims 14 and 15 is acknowledged.

### ***Specification***

2. The previous objections to the specification are withdrawn in light of the Applicant's amendment dated 4/17/2006.

### ***Claim Objections***

3. The previous objections to the claims are withdrawn in light of the Applicant's amendment dated 4/17/2006.

### ***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 8 recites the limitation "the second charge elimination region" on line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of 35 U.S.C. 102(b) which forms the basis for all obviousness rejections set forth in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawajiri et al. (Japanese Patent 2002-134729).

Regarding claim 1, Figs. 10 and 11 of Kawajiri et al. disclose a solid-state imaging device equipped with plural unit pixels (plural pixels can be seen in Fig. 10) each of which includes a photo-diode (15a and 17) and a photo-detector (all features to the left of the aforementioned photodiode in Fig. 11) on a substrate 11, the photo-diode comprising a charge generating region 15a to generate charges upon light irradiation (Paragraphs 6 and 29), the photo-detector comprising a charge accumulation region (15b and 25) to accumulate the charges transferred from the charge generating region (Paragraph 7) and a charge transfer region (portion of 32a disposed between 15a and 15b) provided between the charge generating region and the charge accumulation region (see Fig. 11) of the pixel.

The claims to the generation of a signal potential that changes in accordance with the amount of the charges in the charge accumulation region and claims to the charge transfer region forming a first potential barrier to the charges in the charge generating region and the first potential barrier being removable according to an applied voltage to the photo-detector are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Kawajiri et al. meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Regarding claim 2, Figs. 10 and 11 of Kawajiri et al. disclose the solid-state imaging device according to claim 1, further comprising a first charge eliminating region 32b formed between the substrate 11 and the charge accumulation region (15b and 25).

The claim to the charges in the charge accumulation region being eliminated to the substrate via said first charge eliminating region when a certain voltage is applied to the photo-detector is a purely functional limitation. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Kawajiri et al. meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Regarding claim 3, Figs. 10 and 11 of Kawajiri et al. disclose the solid-state imaging device according to claim 1, further comprising:

- a second charge eliminating region 41 formed near the charge generating region 15a; and
- a region 17c, provided between the charge generating region 15a and the second charge eliminating region 41.

The claims to the region forming a second potential barrier to the charges in the charge accumulation region and the second potential barrier being lower than the first potential barrier such that the charges in the charge eliminating region are overflowed to a surface side, opposite to the substrate, via the second charge eliminating region are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Kawajiri et al. meets the structural

and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Regarding claim 4, Figs. 10 and 11 of Kawajiri et al. disclose the solid-state imaging device according to claim 1.

The claim to the second potential barrier being removable according to an applied voltage to the second charge eliminating region is a purely functional limitation. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Kawajiri et al. meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Regarding claim 5, Figs. 10 and 11 of Kawajiri et al. disclose the solid-state imaging device according to claim 1, wherein the charge generating region 15a has one conductive type (p), same as the substrate 11, and the photo-diode (15a and 17) comprises a first region 17 with opposite conductive type (n) that contacts the charge generating region 15a, and wherein the photo-detector (all features to the left of the aforementioned photodiode in Fig. 11) is a field effect transistor (see Fig. 11) and comprises:

a channel region 17b formed on the surfaces of the charge accumulation region (15b and 25) with one conductive type (p) and the charge transfer region (portion of 32a disposed between 15a and 15b) with opposite conductive type (n);

a gate electrode 19 formed on a gate insulation layer 18 that is formed on the channel region 17b;

a source region 16 having opposite conductive type (n), the source region 16 near the charge accumulation region (15b and 25) being connected to the channel region (see Fig. 11); and

a drain region 17a with opposite conductive type (n) that is apart from the source region 16 by the channel region (see Fig. 11).

The claim to the signal potential being generated in the source region is a purely functional limitation. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Kawajiri et al. meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 6–9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawajiri et al. in view of Miida (U.S. Patent 6476371).

Regarding claims 6 and 7, Figs. 10 and 11 of Kawajiri et al. disclose the solid-state imaging device according to claim 5, wherein the plural pixels are arranged in first

(vertical) and second (horizontal) directions to form a matrix (see Fig. 10) and further comprising:

a first charge eliminating region (Kawajiri et al., Fig. 11 (32b)) formed between the substrate (Kawajiri et al., Fig. 11 (11)) and the charge accumulation region (Kawajiri et al., Fig. 11 (15b and 25)).

Kawajiri et al., however, fails to disclose the switch circuit capable of electrically connecting and disconnecting the source region and the drain region of the pixel and the source regions of the pixels along the first direction being connected to one another, the gate electrodes of the pixel along the second direction being connected to one another and the drain regions of all pixels being common.

Miida teaches a similar semiconductor device wherein there is a switch circuit capable of electrically connecting and disconnecting the source region and the drain region of the pixel (Miida, Col. 8, Lines 22-27 and 46-49); and

the source regions of the pixels along the first direction are connected to one another (Miida, Col. 8, Lines 2-5), the gate electrodes of the pixel along the second direction are connected to one another (Miida, Col. 7, lines 58-60) and the drain regions of all pixels are common (Miida, Col. 7, Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the switch circuit and configuration of Miida into the device of Kawajiri et al. The ordinary artisan would have been motivated to modify Kawajiri et al. in the above manner for the purpose of reading out a video signal that does not contain

a noise component due to the remaining charges from a signal output circuit (Miida, Col. 8, Lines 8-14).

The claims to the charges in the charge accumulation region being eliminated to the substrate via the first charge eliminating region when the potentials of the charge accumulation region and the charge transfer region are increased by boosting up a voltage to the gate electrode and wherein the voltage to the gate electrode is boosted by applying a voltage to the source and drain regions simultaneously while keeping the gate electrode at a high impedance state are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Kawajiri et al. and Miida meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Regarding claim 8, Kawajiri et al. and Miida disclose the solid-state imaging device according to claim 6, wherein a second charge eliminating region (Kawajiri et al., Figs 10 and 11 (41)) has one conductive type (p); and

a second region (Kawajiri et al., Figs 10 and 11 (17c)) with opposite conductive type (n), provided between the charge generating region (Kawajiri et al., Figs 10 and 11 (15a)) and the second charge eliminating region (Kawajiri et al., Figs 10 and 11 (41)) (see Fig. 11 of Kawajiri et al.).

The claims to the second region forming a second potential barrier to the charges in the charge accumulation region and the second potential barrier being lower than the first potential barrier such that the charges in the charge eliminating region are

overflowed to a surface side opposite to the substrate, via the second charge eliminating region are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Kawajiri et al. and Miida meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Regarding claim 9, Kawajiri et al. and Miida disclose the solid-state imaging device according to claim 8.

The claim to the second potential barrier being removable according to the applied voltage to the second charge eliminating region is a purely functional limitation. It is well known that similar structures have similar characteristics and functions.. Thus, as the device of Kawajiri et al. and Miida meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

#### ***Allowable Subject Matter***

7. Claims 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The closest prior art (Kawajiri et al.) does not teach the second charge elimination region being a p+ type impurity region formed on an upper surface of an n+ type impurity region in the photodiode in combination with the additionally claimed

features, as is claimed by the Applicant. Thus, the Applicant's claims are determined to be novel and non-obvious.

### ***Response to Arguments***

8. Applicant's arguments filed with respect to functional language in the claims have been fully considered but they are not persuasive. The Applicant argues that the functional language must be given patentable weight, and that functional limitations have been expressly approved in many cases. The Applicant next cites to a variety of case-law and then further argues (based on *In re Swinehart and Sfiligoj*, 169 USPQ 226 (CCPA 1971)) that functional language is "allowed in claims and is entitled to full weight in claim analysis".

The Examiner argues that, while it is clear from *In re Swinehart and Sfiligoj* that functional language is allowed in claims, the functions themselves (as defined by the functional language) do not cause a claim distinguish over the prior art. As the court in *In re Swinehart and Sfiligoj* stated, "It is elementary that the mere recitation of a newly discovered function or property, inherently possessed by things in the prior art, does not cause a claim drawn to those things to distinguish over the prior art". Therefore, as stated in the above rejection, as the functional limitations can be considered to be inherent properties of the prior art, they are not cause for a patentable distinction to be drawn between said prior art and the instant claims.

Applicant's other arguments have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Kraig whose telephone number is 571-272-8660. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WFK  
05/25/2006

EUGENE LEE  
PRIMARY EXAMINER  
